Novel applications of and solutions in the SOI technology

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The Silicon-On-Insulator (SOI) wafer comprises a single crystal silicon layer (device layer) situated on the supporting silicon wafer (handle wafer), both being separated by a dielectric layer. The electrical insulation of the devices from the handle wafer reduces parasitic capacitances, leakage currents, temperature dependent performance degradation and occurrence of latchup. As the consequence, SOI has allowed making the electronic devices and integrated circuits smaller, faster, and more powerful for already a few decades. While typical applications utilize the insulating function of the oxide in the SOI structure, here we present a novel, alternative way of taking the advantage of SOI – utilizing the extraordinary accuracy of thickness control.

There are types of electronic devices whose performance strongly depend on the final thickness of the die. For example the device efficiency of IGBT technologies increases as the die gets thinner. In order to guarantee the performance stability, however, the thickness must be controlled within limits, which become tighter for thinner dies. The SOI approach offers the solution for new IGBT generations where standard manufacturing technologies are no longer sufficient.

The BGSOI technology (Direct Bond and Grind-back SOI) - the basic method of making SOI wafers – will do the trick for reasonable price. After wafer bonding and bond strengthening annealing, the material of the device wafer is removed by means of mechanical grinding and the surface of the final device layer is finished by polishing. The typically achievable uniformity of the device layer thickness is $\pm$ 0.5 μm. The material of the supporting wafer is removed by Taiko grinding and silicon etching and the buried oxide is removed by HF etching. The resulting die thickness keeps the exceptional thickness uniformity of BGSOI, which is an order of magnitude better compared to conventional variability of Taiko grinding ($\geq \pm$ 5.0 μm) used with conventional process of device manufacturing.

Novel solutions of aspects specific for SOI are discussed as well. These include gettering and stress engineering.

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