Gettering techniques for SOI wafers

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The Silicon-On-Insulator (SOI) wafer consists of a handle wafer and a device layer, both being separated by a dielectric isolation. The handle wafer usually serves as the supporting layer only with no influence to device parameters. The device layer (made from silicon single crystal) has the thickness ranging from less than one micrometer for "thin SOI" up to more than ten micrometers for "thick SOI". The electrical insulation is usually less than one micrometer thick silicon dioxide layer which helps to reduce parasitic capacitances, leakage currents and temperature dependent performance degradation. The SOI concept allows making the electronic devices and integrated circuits smaller, faster, and more powerful. On the other hand, solution of heat dissipation or impurity gettering is more complicated than for standard silicon wafers.

The presence of the buried oxide layer prevents diffusion of contaminants from the device layer to the bulk of the handle wafer and to the wafer backside. The gettering sinks are therefore preferentially placed between the buried oxide and the device layer or on the top of the device layer. However, the close proximity of the gettering sinks to the devices induces some restrictions and requirements to the gettering techniques used. The solution may vary for thin and thick SOI.

The overview of the gettering techniques used for SOI wafers will be presented and the need for novel solutions will be discussed.